UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,934	07/07/2003	Takehiro Shimizu	H-1098	6928

7590	12/15/2005

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EXAMINER
CODY, DILLON J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/612,934	SHIMIZU ET AL.
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 July 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>07 July 2003</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>7 July 2003</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 7-05)   Office Action Summary   Part of Paper No./Mail Date 20051123

DETAILED ACTION

1.   Claims 1-20 are pending.

Papers Filed

2.   Examiner acknowledges receipt of claims, specification, abstract, drawings,

declaration, and information disclosure statement, all received 7 July 2003.

Information Disclosure Statement

3.   The information disclosure statement filed 7 July 2003 fails to comply with the

provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because Japanese patent documents

AM, AN and AO failed to include an English language translation of the abstract. It has

been placed in the application file, but information referred to therein has not been

considered as to the merits. Applicant is advised that the date of any re-submission of

any item of information contained in this information disclosure statement or the

submission of any missing element(s) will be the date of submission for purposes of

determining compliance with the requirements based on the time of filing the statement,

including all certification requirements for statements under 37 CFR 1.97(e). See

MPEP § 609.05(a).

Title

4.   The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

Drawings

5.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "170" has been used to designate both "Address Array" and "Data Array" in Fig. 10. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6.   The disclosure is objected to because of the following informalities:

Page 2, line 5: "microprocessor" should read "microprocessors"

Page 2, line 19: the comma after "because" should be removed

Page 5, line 19: "had" should read "has"

Page 5, line 22: the semicolon after "buffer" should be a comma

Page 13, line 17: "BIU102" should include a space between "BIU" and "102"

Page 13, line 17: "op121" should read "121"

Appropriate correction is required.

7.   The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

8.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9.   Claim 7 recites the limitation "said instruction" in line 4 and claim 9 line 5. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether "said instruction" refers to the instruction of claim 1 or the instruction immediately disclosed on line 3 of claim 7 and line 3 of claim 9. The examiner will assume it refers to the instruction of claim 1 for purposes of examination.

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act

of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior

to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11.   Claims 1-6 and 10-20 are rejected under 35 U.S.C. 102(e) as being anticipated

by Augsburg et al. (U.S. Patent No. 6,948,053) hereinafter referred to as Augsburg.

12.   As per claim 1, Augsburg discloses a data processing device, capable of

decoding and executing instructions, comprising: a cache memory (Fig. 2 instruction

cache 203) where said instructions are held, wherein said instructions each contain a

spare field (Fig. 6 bit 601), and wherein said cache memory holds information which is

generated according to predecoding of instructions in a first corresponding area

corresponding to said spare field. (Col. 3 lines 18-23) *The examiner asserts that field*

601 is a spare field. Before an instruction is predecoded, nothing exists in the bit

following the displacement of a conditional branch instruction (as in Fig. 5), rendering

the bit field a spare field.

13.   As per claim 2, Augsburg discloses the data processing device according to

claim 1, further comprising: controlling means (Fig. 2 decoder/sequencer 204) which

controls an executing sequence of said instructions based on information of said spare

field, when executing instructions loaded from said cache memory. (Col. 6 lines 28-48)

The examiner asserts that the decoder uses the carry bit stored in the spare field to

calculate the physical address of the branch target instruction.

14.   As per claim 3, Augsburg discloses the data processing device according to

claim 2, further comprising: a predecoder (Fig. 2 unit 202) which predecodes said

instructions to generate said information before instructions are stored into said cache

memory. (Col. 5 lines 46-64)

15.   As per claim 4, Augsburg discloses the data processing device according to

claim 3, wherein said predecoder (Fig. 2 unit 202) decodes operation codes contained

in first fields of said instructions. (Col. 5 lines 46-64) *The examiner asserts that the*

opcode occupies the first fields of an instruction as pictured in Fig. 5 and described in

col. 9 line 9-12. Further, the predecoder decodes the opcode to determine if the

instruction is a branch instruction. (Col. 8, lines 54-57)

16.   As per claim 5, Augsburg discloses the data processing device according to

claim 4, wherein information on a type of instruction obtained from decoding results

from said predecoder is held in said first corresponding area of said cache memory.

The examiner asserts that decoding a branch instruction includes calculating a portion

of the effective branch target address and storing it in the instruction. Further, the carry

bit is stored in the spare field as a part of this decoding. The presence of the carry bit

indicates a branch instruction, as no other type of instruction uses the spare field in

predecoding.

17.   As per claim 6, Augsburg discloses the data processing device according to

claim 5, wherein said type of instruction includes an information of whether said

instruction is a branch instruction or not. *The examiner asserts that the presence of the*

carry bit indicates a branch instruction, as no other type of instruction uses the spare

field in predecoding.

18.   As per claim 10, Augsburg discloses the data processing device according to

claim 3, further comprising: a processor performing calculations using information

contained in first fields of said instructions before storing said instructions in said cache

memory. (Col. 5, lines 46-64) *The examiner asserts that the encoding unit 202 uses*

opcodes to determine whether the instruction is a branch instruction (Col. 8 lines 54-57),

and hence, if the displacement should be used to calculate a physical address.

19.   As per claim 11, Augsburg discloses the data processing device according to

claim 10, wherein based on said decoding results, said cache memory holds calculation

results from said processor in a second corresponding area of said instruction cache

memory corresponding to said first fields. (Col. 5 lines 46-64)

20.   As per claim 12, Augsburg discloses the data processing device according to claim 10, wherein to handle relative branch instructions of program counters with n bit displacements, said processor adds information of n lower bits of addresses of said program counters for displacements of said first fields in an adding operation, and wherein added results by said processor are held in said second corresponding area of said cache memory, and wherein carry information of said adding operation is held in said first corresponding area. (Col. 5, lines 46-64)

21.   As per claim 13, Augsburg discloses a data processing device, capable of decoding and executing instructions, comprising: a cache memory (Fig. 2 instruction cache 203) where said instructions are held; and a predecoder (Fig. 2 unit 202) which performs predecoding of said instructions before said instructions are stored in said cache memory, wherein said cache memory holds information (Fig. 6 field 601) generated by said predecoding of said instructions in an area which has a one to one relation with said instructions. (Col. 5 line 65-67)

22.   As per claim 14, Augsburg discloses the data processing device according to claim 13, further comprising: controlling means (Fig. 2 decode/selecting unit 204) which controls an executing sequence of said instructions based on said information, when executing instructions are loaded from said cache memory. (Col. 6 lines 28-42) *The examiner asserts that the carry bit stored in field 601 is used in calculating a branch target address, which is used in controlling the flow of the processor.*

23.   As per claim 15, Augsburg discloses the data processing device according to

claim 14, wherein said area is an area corresponding to a spare field of an instruction.

The examiner asserts that since field 601 is not used until the instruction has been

predecoded by the encoder, the field constitutes a spare field.

24.   As per claim 16, Augsburg discloses a data processing device, capable of

decoding and executing instructions, comprising: a cache memory (Fig. 2, instruction

cache 203); and a predecoder (Fig. 2 encoding logic unit 202), wherein when an

instruction is loaded, information generated from predecoding an instruction code of

said instruction by said predecoder is written to a first area (Fig. 6 field 601) in said

cache memory, and wherein said first area corresponds to a spare field of said

instruction code.   *The examiner asserts that when an instruction is decoded to be a*

branch instruction, a carry bit is written to field 601 depending on the physical address

calculation carried out in the encoding logic unit. (Col. 5 lines 46-64)

25.   As per claim 17, Augsburg discloses the data processing device according to

claim 16, further comprising: a bus interface unit (Fig. 1 North Bridge 103) controlling

input and output of data, wherein said instruction is loaded from an external memory

(Fig. 1 memory 102) through said bus interface circuit to said cache memory (Fig. 2

instruction cache 203), and wherein data from said bus interface unit to said cache

memory flows through said predecoder (Fig. 2 encoding logic unit 202) for precoding.

The examiner asserts that the North Bridge interfaces the processor to the bus, as

depicted in Fig. 1 (Col. 4 line 31-34)

26. As per claim 18, Augsburg discloses the data processing device according to

claim 17, wherein when said data processing device executes instructions loaded from

said cache memory, said information stored in said first area is used. *The examiner*

asserts that the carry bit is used in execution of an instruction, specifically in calculating

the physical branch target address. (Col. 6 lines 28-42)

27. As per claim 19, Augsburg discloses the data processing device according to

claim 18, wherein said information stored in said first area includes an information on

branching. *The examiner asserts that the carry bit pertains to branching, specifically to*

the branch-to address.

28. As per claim 20, Augsburg discloses the data processing device according to

claim 19, further comprising: a floating point operation unit (Fig. 2 floating point unit

206); and a data cache memory (Fig. 2 data cache at bottom of diagram).

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

30.   Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Augsburg

in view of Nishimukai et al. (U.S. Patent No. 4,912,635) hereinafter referred to as

Nishimukai.

31.   Augsburg discloses the data processing device according to claim 6.

32.   Augsburg fails to disclose said controlling means commands fetching an

instruction of a branched place, when it determines that said instruction is a branch

instruction according to said information in said first corresponding area of said cache

memory.

33.   Nishimukai discloses fetching an instruction of a branched place, when it

determines that said instruction is a branch instruction. (Col. 2 line 65 – col. 3 line 9)

34.   Nishimukai discloses that his invention "can shorten the branch instruction

executing time" (Col. 1 line 13-14), which is a desired effect in Augsburg's invention.

35.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have combined Nishimukai's method of fetching a branch target instruction

upon decoding a conditional branch instruction for the benefit of shortened branch

instruction processing time.

36.   Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Augsburg in view of Nishimukai, in further view of Irie et al. (U.S. Patent No. 6,499,712)

hereinafter referred to as Irie.

37.   As per claim 8, Augsburg in view of Nishimukai disclose the data processing

device according to claim 7, further comprising:

      a queuing buffer temporarily storing instructions loaded from said

instruction cache memory (Augsburg Fig. 2 decode unit 204) *The examiner*

asserts that an instruction is temporarily stored in the decoder after being fetched

from the instruction cache;

      and a target buffer (Nishimukai's index and data fields inside his

associative memory) which holds an address of said branched place, said

instruction of said branched place, and a following address of said address of

said branched place, *The examiner asserts that in the example beginning in*

Nishimukai's col. 5, instruction 10 is the instruction of said branched place and its

address and the address of instruction 11 are both stored in index fields of

associative memory 10. Instruction 11's address is a following address of

instruction 10's.

38.   Augsburg and Nishimukai fail to disclose dividing one branch operation into a

prepare target instruction and a branch procedure instruction, wherein said prepare

target instruction commands the calculations of said address of said branched place

and fetching of said instruction of said branched place, wherein said branch procedure

instruction commands branch condition checks and branch procedures.

39.   Irie discloses dividing one branch operation into a prepare target instruction and

a branch procedure instruction, wherein said prepare target instruction commands the

calculations of said address of said branched place and fetching of said instruction of

said branched place, wherein said branch procedure instruction commands branch

condition checks and branch procedures. (Col. 9 lines 40-56)

40.   Irie discloses low-penalty branching (Col. 9 lines 40-43) which is well-known in

the art to decrease pipeline stalls and processing time. Increased processing

performance is a goal of Augsburg's and Nishimukai's inventions.

41.   It would have been obvious to one of ordinary skill in the art at the time of

invention to include Irie's method of splitting branch instructions into prepare-target

instructions and branch operation instructions in Augsburg's decode unit for the benefit

of reducing branching penalties, and therein increasing processing performance.

42.   As per claim 9, Augsburg in view of Nishimukai and Irie disclose the data

processing device according to claim 8, wherein said controlling means issues

commands to load said instruction of said branched place and said following address

from said target buffer when said controlling means determines that said instruction is a

branch procedure instruction according to said information of said queuing buffer which

was loaded from first corresponding area of said cache memory. *The examiner asserts*

that when the decoder has determined the branch target address using Augsburg's

carry bit, it can fetch Nishmukai's instruction 10 (Col. 8 lines 7-14) and use the address

of instruction 11 to load instruction 11 (Col. 8 lines 34-35).

Conclusion

43.   The following is text cited from 37 CFR 1.111(c): In amending in reply to a

rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments

avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dillon Cody whose telephone number is 571-272-8401.

The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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